Opportunities and Solutions in Patterning LED's.

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Abstract
The literature on high brightness LED's shows that patterning the top surface of LED's with photonic crystals is being used to create the most intense LED light sources. The best example is that you can now buy projection displays that are illuminated by LED's with Photonic Crystals.

The experimental and model data, reviewed in this article, shows that patterning delivers value through improved beam shaping and light extraction using carefully optimized photonic crystals. The data also suggests that in the future, patterning in combination with sub micron device layers and strategically placed mirrors can produce extraction efficiencies of greater than 80%. In addition, patterning can improve current spreading and reduce epitaxy defects. The long term goal is to develop a LED that can be used with minimal additional packaging to focus the light or extract heat.

The solution to low cost patterning for Photonic Crystals with 100 nm features is to use imprint. The imprint patterning process is implemented in a module that consists of a clean and coat tool, an imprint tool and an etch tool. Cleaning is essential because imprint is a contact technology and particles will lead to process defects and mold damage. There are 2 companies that are developing production tools for LED applications; Molecular Imprints (MII) and Obducat. There are 2 companies that are supporting research tools, and expect to develop production systems in response to customer order, EV Group and Nanonex. The principal difference between imprint suppliers are the different strategies used to conform the mold to the substrate, and the state of system development. To date MII has published the most complete process performance data on an automated production tool. The cost of patterning is less than 0.5 cent per device.

First the value of increased LED output will be described, followed by a discussion of the different patterning solutions for improving output, then the different solutions for creating the patterning will be described and finally the costs are estimated.

1. Value
Light Emitting Diodes (LED’s) are projected to have a major impact on the world’s energy consumption. We spend $230 B world wide on lighting and if the projected 30% savings come to pass, then the world will need approximately 300 fewer power plants and the fuel they use¹. These numbers impact national planning and are a great opportunity to affect green house gas emissions. As a result there are major government programs on advanced LED’s in many countries to both take advantage of the energy savings and become the world wide leaders in this new technology. Today’s LED is as efficient a source as florescent, has 5 x the life and 5 x the cost. LED’s are being used in high maintenance and low power applications.

The drive to improve efficiency of LEDs has a significant impact on cost of the package. Similar to many integrated circuits, the cost of the package in LED’s is over 50% of the device cost. Today’s LED’s require large heat sinks to keep them cool, which also adds to the cost of the package. Improvement in LED efficiency will allow larger die in lower cost packages.

The target Cost of Ownership (CoO) must be consistent with a typical die value of 10 cents per device and 8000 devices per wafer, or a total of $800 a wafer. A cost add of less than $20 or 2.5% a wafer should be acceptable, in exchange for significant improvements in LED output from 1.2 to 2x and control of beam shape.
2. Traditional extraction solutions

The root cause of the extraction problem is that the light is emitted inside a high refractive index semiconductor that acts as a waveguide, trapping light by Total Internal Reflection, so that only 8% of the light is extracted (Figure 1a).

![Diagram](image)

**Figure 1 Light emission from a) a planar (left) and hemispherical encapsulated LED (right), the curve surface of the encapsulation eliminates total internal reflection at the air encapsulant interface.**

- **Encapsulation**

The problem of extraction could be solved immediately if a large hemispherical dome of material index matched to GaN could be created. This would eliminate all TIR at surface of the device. Unfortunately growing and etching the additional millimeters of material is cost prohibitive. The first solution, used on the very earliest LED’s, is to encapsulate the LED in a hemispherical epoxy package with a low refractive index of around 1.5 (Figure 1b). Virtually all the light that makes it through to the encapsulant is transmitted by the curved surface and 32% of the light is extracted from a mirrored LED. The downside of this approach is the cost of packaging and limited life of the epoxy, especially critical for high power applications.

There are additional problems when a hemispherical encapsulation is used for imaging applications. The larger the outer dimensions of the encapsulation become, the greater the spot size of the source. This significantly reduces the point source brightness of the LED.

- **Edge Facets**

One very costly, but effective way, to extract the light from the waveguide is to facet the edges of the die as shown in Figure 2a. Each die must be custom machined and polished. This is an expensive process and not suitable for mass production but can produce IR LED’s and high power GaP devices with external quantum efficiencies of >50% and extraction efficiencies close to 75% (when operating in pulsed mode). Osram has produced red devices in which the active area is divided into sections with angled walls to reflect the waveguided modes - called a “micro-mirror LED”, as shown in Figure 2b. The light output per die is reduced due to the significant loss of active area, that could be as high as 30-50%. It is not clear that this technology has been reduced to commercial products.
Figure 2 Faceted LED’s for improved extraction a) Schematic and b) picture of a truncated inverted pyramid LED reported by Lumileds \(^5\). c) Micromirror LED with angled mirrored recesses in the active layer \(^6\).

Roughening top surface

It is generally recognized that the most common extraction technique is to roughen the surface, so that any light that meets the roughened surface is scattered out rather than reflected back (Figure 3). The scattered light forms a random or “lambertian” scattering pattern. Data on roughening shows 12-20% extraction efficiency \(^7\) \(^8\) \(^9\). This is a relatively low cost process; however, control and repeatability have been described as the limitations of this solution.

Figure 3 A cross-section of roughened LED, showing lambertian light distribution \(^6\).

Surface roughened LEDs that are then combined with encapsulation appear to be the process of choice for many high brightness LED’s. There is very little published data on the combined effect; presumably this is due to commercial sensitivity.

3. Photonic crystals

Photonic Crystals can improve extraction efficiency and beam shaping in LED’s. Classic Photonic Crystals (PC) are regular sub-wavelength variations in refractive index that extend all the way through a waveguide (Figure 4a)\(^10\). In practice, it is difficult to make the holes pass through the quantum well in the LED because the holes will reduce the emitting area and will provide surface recombination sites. As a result the PC in a LED is usually limited to the surface and behaves more like a diffraction grating. A typical LED cross-section is shown in Figure 4 b\(^11\).

There are two types of 2D photonic crystals; regular lattice and Photonic Quasi Crystals. The regular lattice is shown in Figure 5a, and consist of a regular array of holes laid out in a rectangular or triangular array. A quasi crystal lattice is shown in Figure 5b where there is no short range order, but there is circularly symmetric long range order.

Mesophotonics have developed a model and Intellectual Property for Photonic Quasi Crystals (PQC) on LED’s\(^12\). PQC represent a particular challenge because the simulation must take account of the non repeating unit cell. Some examples of the effects of varying the parameters of the P(Q)C on the spatial cross-section are shown in Figure 6a. The profiles in Figure 6a show that the shape of the light distribution can be engineered by varying the parameters of the crystal. In all cases except those on the far right, the majority of light is extracted in a cone within 30 degrees of normal.
Figure 4 Schematic of a Photonic Crystal (PC)  a) classic PC that penetrates waveguide, b) a practical implementation on surface of LED.  

Figure 5 Different photonic crystal lattice designs a) SEM of regular and b) schematic of quasi crystal pattern, c) example of a Photonic Quasi Crystal pattern, courtesy of MII.  

The radial profile in Figure 6b shows that the regular crystal (blue line) produces lobes corresponding to the axes of the crystal. In comparison, the quasi crystal (red line), produces radially uniform output due to the circularly symmetric Photonic Quasi Crystal (PQC). The PQC is essential to obtain uniform output LED's for illumination applications or phosphor based LED's. Beam shaping in general, and increased spot intensity in particular, is the reason for the early adoption of PC on LED's.
Extraction can be further improved by placing a metal layer close to the Multiple Quantum Well (MQW) forming a “microcavity”. SemiLEDs introduced devices with a metal reflector and a patterned surface with “photon-injecting nozzle” microstructures to enhance light extraction (Figure 7a). Published data from Lumileds is shown in Figure 7b, where the position of an underlying conductor can increase the light extraction to 60% in this sort of “micro-cavity”.  

**Quantitative comparison on Photonic Crystals with traditional solutions**

The data on extraction for the different extraction techniques can now be consolidated. Most of the publications reported their results as an increase over a flat die, and avoid the challenges of making a reliable absolute light measurement. In this consolidation, the flat die reference conditions were chosen to be GaN with an extraction of 8% from one side with the opposite side a mirror. The experimental data from the best optimized devices is combined with models, and is shown in Figure 8a and b.
The consolidated data shows that:

- Roughening (R), PC and PQC are equivalent in total extraction.
- Microcavity LED with a mirror within 1 wavelength of the MQW have a significant impact increasing output by 1.7x.
- The model and the best optimized experimental data for roughened, PC and PQC are in good agreement and can achieve 60% extraction with encapsulation.
- The model data for the ultra-thin LED device, less than 0.5 um thick, provides the ultimate opportunity and will be discussed in the next section.
- For light into a 30 degree cone, the P(Q)C increases output by 2 x compared to flat LED. Encapsulation is not a practical solution for imaging applications because of its limited life in high power LED’s.

In particular, the improved light into a 30 degree cone and the improved uniformity with Photonic Quasi Crystals are both key enablers for imaging applications.

Potential for ultra thin LED’s

The current trend in device design is towards ultra thin LED’s that attempt to manage the waveguide modes when combined with strategically placed mirrors to maximize extraction. Combining metal layers with waveguide management have led to modeling evaluations of what might be possible in ultra thin LED’s. Hershey 19 used a waveguide model on a waveguide that included a 100 nm thick MQW and a light extraction layer with 80% the refractive index of the semiconductor, equivalent to a Photonic Crystal (Figure 9). The presence of multiple layers affects the waveguide modes. For example the MQW controls the location of the zero order (Figure 9a). As the device is thinned the optical energy or intensity of the light in more of the guided modes is forced into overlap with the light extraction layer (Figure 9 b-d). The result of thinning is seen on extraction data from full simulations shown in Figure 10. Details of simulations reported in patent specifications suggest that ultra-thin GaN devices with mirrors and carefully optimized quasi crystal patterns can get >80% extraction 13.
Figure 9 The effect of thinning LED on waveguide modes in the presence of Quantum layers and light extraction layers \(^{16}\). a) 4 um thick GaN heterostructure with 100 nm thick MQW, and photonic crystal light extraction layer with the 3 lowest orders shown. b)-d) 600 nm to 400 nm thick layers showing the increased overlap of the orders with the light extraction layer.

![Figure 9](image)

Figure 10 Extraction relative to a flat LED for LED’s of different thicknesses. The Photonic Crystal design was optimized for GaN thicknesses of 1.5 um and fixed for the remaining simulations. The efficiency improves sharply for devices less than 500 nm thick \(^{12}\).

The future of high brightness LED’s seems to be headed towards these ultra thin devices, the key is to get the electrical properties right and manufacturing costs down. Low cost patterning is a crucial element of cost controls. There are other opportunities for patterning in improving current spreading using webs of conductors, and in lateral overgrowth epitaxy.

4. Imprint patterning solutions.

The requirements for patterning on LED’s are as follows:

<table>
<thead>
<tr>
<th>Requirements</th>
<th>LED</th>
<th>Integrated circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature size</td>
<td>100 nm hole 200 nm pitch</td>
<td>45 nm lines and spaces</td>
</tr>
<tr>
<td>Overlay</td>
<td>None to 2-3 um, depending on design</td>
<td>15 nm</td>
</tr>
<tr>
<td>Defect sensitivity</td>
<td>&lt;0.1% of device area (5x5 um)</td>
<td>45 nm defects are device lethal</td>
</tr>
<tr>
<td>Tolerance to substrate flatness</td>
<td>&gt; 10 um</td>
<td>&lt; 10 nm</td>
</tr>
<tr>
<td>COO</td>
<td>&lt;$20 per wafer</td>
<td>&lt;$50</td>
</tr>
</tbody>
</table>

The LED application is much more relaxed than IC’s for overlay and defect density. However the challenge is in the substrate surface flatness which is highly variable. The wafers are non flat due to incoming quality of low priced substrates, bowing from high temperature epitaxy growth on substrates with significant thermal expansion coefficient mismatch, and hillocks or nodules from epitaxy defects. The non flatness varies widely with vendors and process, but a few studies have been published.
The characteristics of wafers before and after epitaxy have been reported by a team from Hitachi\textsuperscript{20,21} for different length scales. Examples of their data are shown in wafer bow of 50 um in Figure 11a and a roughness of 150 nm after epi in Figure 11c. Wafer bow can be reduced 5x by appropriate wafer chucking.

Figure 11 Wafer quality a) Bowing of sapphire wafers after epi growth of 2 um of GaN. The interferograms are shown at top and height profile in the x axis are shown below, with 40-80 um of bow\textsuperscript{21}. Surface topography scans of SiC wafers before b) and after epi c) showing 100-150 nm of additional surface variation.\textsuperscript{20}

There are a number of possible patterning solutions; optical, electron beam, and imprint lithography. The optical deep UV step and repeat lithography requires very flat wafers because of their shallow depth of field (<200 nm), so the non flat LED wafers cannot be patterned reliably by optical imaging. Regular lattice Photonic Crystals have been fabricated by interferometric lithography, and is known to be challenging to maintain process stability. Electron beam direct write is too slow and expensive. LED’s are an ideal application for imprint because of their need for very small features, with limited overlay and defect density requirements.

Imprint lithography is a molding technique. In its simplest implementation, the mold has a relief pattern which is pushed into a liquid coating on a wafer (Figure 12a). The liquid is then UV crosslinked to set the pattern, and the mold pulled away to separate as shown below. Drop dispense allows liquids with “water – like” viscosity to be used. The multiple process steps form an imprint module as shown Figure 12b along with examples of typical process equipment in Figure 13.
5. Mold Fabrication

For features less than 400nm, the original master mold is created by direct write electron beam lithography, followed by dry etch of a chrome layer that then acts as the “hard mask” for etching the substrate. The cost is dependent on the write time which in turn depends on the feature size and write area. The alternatives are illustrated in Figure 14.
Figure 14 Making the mold. The process starts with either electron beam direct write of either a few die or a whole wafer area of an original pattern. The original of a few die is step and repeat imprinted (S&R) to create a whole wafer area. The whole wafer mold can either be used directly or copied into multiple working plates.

The standard approach to producing the original pattern is to write the whole wafer. Molecular Imprints have reported writing a smaller area of 5x5 mm and then using their step and repeat imprint tool to pattern the whole wafer area.

Once you have a master that covers the whole area, this can be used for imprint, or alternatively daughters (working plates) can be fabricated. In the case of soft plastic molds, a large number of working plates are needed, so a critical issue for any LED manufacturers are sources for working plates.

The overall mold cost should be reduced by using the step and repeat approach. The cost of using daughters depends on working plate life and cost.

6. Mold conformality
The imprint vendors have different mold strategies to manage wafer non-flatness.

- Imprint while relying on the flexing of the wafer to conform to a thick glass mold. This is the old contact printer solution that cannot deal effectively with LED wafers.
- Imprint using a conformal hard thin glass mold used by MII and Nanonex
- Imprint using a flexible 2 layer polymer mold used by EVG
- Imprint using a “one use” plastic film mold that is itself imprinted in parallel with the wafer used by Obducat.

**Thin hard glass molds**
MII have reported on their production system based on thin glass molds (Figure 14a) to conform to a wafer that is held on a vacuum chuck (Figure 14b). The surface of glass molds are hard which helps both process life and defect density. MII has published extensively on the performance of their automated system, the process and making the molds;

- **Conformality** - on a substrate that was flat to 8 um, the imprinted layer was a single color with a residual layer 23 nm thick and variation 8 nm TIR.
- **Process life** - life of 525 wafers between mold cleans with residual layer variation < 10 nm 3 sigma.
• Mold life - They have also reported that the mold can be cleaned over 30 times without damage, suggesting a mold life of at least 15,000 wafers.
• Defect density - < 0.1 defects per squcm, for defects greater than 0.2 um on molds with sparse resolution test patterns.
• Process type – image reversal bilayer process with 2.5x greater tolerance to residual layer variation as compared to a conventional single layer “direct imprint” process, as will be discussed later.
• Mold manufacture – fabricate a 5x5mm original by commercial electron beam lithography followed by imprint step and repeat to create a low cost whole wafer mold, with a stepping overlay of < 500 nm.

MII plans to supply the thin glass molds needed for their whole wafer system.

Nanonex have reported good pressure uniformity with their “Air Cushion Press”, and have obtained most of their process data with thin glass wafers.

**Two layer plastic molds**

Plastic molds mounted on glass substrates have been widely used in numerous imprint publications. PDMS is the material of choice as it is a soft rubber that conforms and has good release properties. The problem is that for small or high aspect ratio features, the mold tends to deform as shown in Figure 15a.

EVG are recommending a 2 layer PDMS mold solution for LED wafers, the hard surface layer prevents deformation shown in Figure 15b. EVG plans to supply the working plates or support the LED manufacturer to make their own working plates. The process life, sourcing and cost of the daughter molds is a critical question for this solution that has yet to be reported in the open literature. Large particles and surface roughness will damage soft molds, so wafer cleanliness is critical.

**Figure 15** Conformality using a thin glass mold; a) shows the a thin glass mold before imprint, b) shows the mold conforming during imprint (courtesy MII).

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**Figure 16** Three approaches to plastic molds a) raised squares imprinted using a soft PDMS mold that tend to deform during imprint, b) two layer molds with a hard plastic surface, or c) a “one use” hard plastic sheet that travels from top to bottom, and used to imprint wafers traveling from left to right.
One use plastic molds
The materials for a “one use mold” have been supplied by Transfer Devices for several years. Obducat have described a new concept in which the mold creation is integrated into a system. A master mold is used to imprint the surface of a plastic film, which is then used as the working mold to imprint the wafer, a schematic of a 2 headed imprint system is shown Figure 15c. The wafer moves from left to right, starting with coating, followed by imprint and separation. At the same time, a roll of plastic sheet moves from top to bottom. A master mold is used to imprint the bottom of the plastic sheet. The sheet moves over the wafer and is used as a “one use mold” to imprint the wafer.

The advantage is that the working mold is only used once, so damage to the mold from the wafer is not a concern. The imprint quality must still be monitored to check for problems in the first step used to make the working mold. The challenge will be in integrating the additional complexity of two imprint heads and the roll to roll material transport into a reliable production tool. Presumably, the use of a plastic film with a relatively low (1/10th) modulus compared to glass will significantly impact the overlay performance. The first Obducat systems will not support overlay.

7. Process control
Non flatness or roughness with small lateral dimensions will not be managed by conformality, as shown in Figure 17, and must be managed by the process.

Figure 17 A schematic showing the impact of conformality. The left hand sketch shows a rigid template and a non flat wafer where the gaps are all filled by the imprint material and the residual layer variation is equal to the wafer flatness. The right hand sketch shows a flexible mold that conforms to the long length scale variation (L1), but not to the short length scale (L2).

The process margin in the different options can be compared by estimating how much residual layer variation they can tolerate. The simplest process is to imprint into a single layer and then etch away the residual layer, as shown in Figure 18 Schematic showing the impact of residual layer variation on feature size. The feature height must be at least 2 x the MAXIMUM residual layer thickness if the pattern is to survive clearing the residual layer. Any non vertical wall angle will also cause changes in feature size. For a 100 nm feature that is 100 nm high, the MAXIMUM residual layer thickness must be less than ½ the feature height, which means that a typical requirement for residual layer thickness would be 30 nm ± 20 nm, that would produce a maximum thickness of 50 nm and a minimum of 10 nm.

Meeting this spec is extremely difficult. The mean residual layer thickness is controlled by the high spots on the wafer, because of the difficulties of getting liquid to flow away from thin gaps. Published data for spin on UV reports 50-75 nm mean residual layer thickness. Data for low viscosity materials deposited using drop on demand has shown 30 nm mean residual layer thickness on exceptionally flat wafers.

The inevitable conclusion is that robust wafer processing requires either much deeper toothed (200 nm) mold or multilayer process. The deep tooth mold has its own challenges in mold making with controlled wall angle, problems with separation and increasing imprint fill times.
Figure 18 Schematic showing the impact of residual layer variation on feature size. The feature height must be at least 2 x the MAXIMUM residual layer thickness if the pattern is to survive clearing the residual layer. Any non-vertical wall angle will also cause changes in feature size.

To avoid the issues associated with imprinting deep features multi-layer processing can be used to transfer a thin patterning layer into an underlying transfer layer prior to etching. Multilayer processes have been used in CMOS processing for years to improve process margin and CD control. There are two bilayer processes being used, as shown in Figure 19.

In the process in Figure 19a, developed by Grant Willson’s team at U. Texas\textsuperscript{37}, a spin on organic polymer is used as a base layer to planarize the substrate, and then imprinted with a silicon containing material on top. The residual layer is etched through, and then an oxygen plasma is used to etch through the planarizing layer. One challenge is to get the silicon content of the imprint material high enough to be a good etch mask.

An alternative is a bilayer image reversal process, developed by Molecular Imprints and shown in Figure 19b\textsuperscript{38}. The imprint material is organic and a silicon containing material is spun on top. The silicon material is etched back to expose the organic, and then the gas is changed to etch the underlying organic. In this case, the mold naturally planarizes the surface to the point at which the mold conforms. In addition, it is relatively easy to create a high silicon containing spin on material similar to “spin on glass”. As a side effect, the “image” of the imprint is reversed compared to the process on the left.
Figure 19 Schematic of bilayer process options. On the left, a spin on organic material is used as a planarization layer followed by a silicon containing imprint material (SFIL). On the right, the imprint material is organic followed by a spin on silicon layer on top (SFIL/R). In both cases, a fluorine containing etch is used to clear down to the underlying organic, and then an oxygen etch is used to transfer the pattern down to the substrate.

Figure 20 Anisotropic oxygen etching allows transfer of 50 nm features through a planarization layer that varies in thickness by 100 nm. The process used was image reversal with imprint planarization (SFIL/R), courtesy of MII.

The pattern is transferred through the planarization layer by oxygen reactive ion etch. Molecular Imprints have shown 50 nm features patterning through layers varying from 200 to 100 nm thicknesses. The limitation on aspect ratio is the mechanical stability of the feature. For 100 nm features needed for Photonic Crystals, the pattern transfer can work on any layer from 200 to 400 nm thick. For the imprint planarization step, a target specification would be a residual layer of 300 nm ± 100 nm.

Tri layer process can also be used, over the years, numerous examples of tri layer processes that use an intermediate thin hard mask between the planarization layer and the patterned layer have been reported.

The mold depth, conformality and process effects form general design rules, which are summarized in Figure 21. For direct imprint, a minimum mold depth 200 nm is needed and the maximum residual layer variation that can be tolerated is still only ± 40 nm. The image reversal process can tolerate a maximum residual layer variation of ± 100 nm i.e. 2.5 times larger. In these processes, the ability of the process to maintain feature size control is directly related to the size of the process margin.
<table>
<thead>
<tr>
<th>Mold Depth</th>
<th>Imprint Residual Layer Thickness (RLT) Mean</th>
<th>Residual Layer Tolerance</th>
<th>Planarization Layer Variation ±</th>
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<tr>
<td>Direct Imprint</td>
<td>200 nm</td>
<td>&lt;60 nm</td>
<td>± 40 nm</td>
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<tr>
<td>Standard Bi layer (SFIL) or Tri layer</td>
<td>100 nm</td>
<td>&lt;30 nm</td>
<td>± 20 nm</td>
</tr>
<tr>
<td>Image reverse bi layer (SFIL/R)</td>
<td>100 nm</td>
<td>&lt;300 nm</td>
<td>± 100 nm for all lateral dimensions</td>
</tr>
</tbody>
</table>

*Figure 21* Summary of the process design rules for direct imprint and multilayer processing. The image reversal process has significantly greater process window. Direct imprint requires a mold depth of at least 200 nm.

### 7. Imprint Suppliers

The different vendor recommendations can be summarized.

- **EVG** recommends a two layer plastic mold, spin on imprint material, and direct imprint on wafer. The users must deal with the need for multiple working plates and wet wafers. Their solution offers potential process simplicity but unknown process margin. EVG is waiting for orders before developing production tools.

- **MII** recommend a thin hard glass mold made by step and repeat, drop dispense UV imprint material, and a multilayer process. The user must deal with the complexity of a multilayer process. Their solution offers the advantages of highest throughput potential, greatest process margin and documented process capability for feature size control, defect density and process life.

- **Nanonex** avoid specific UV process recommendations, but claim process and system flexibility. They are waiting for orders before developing production tools.

- **Obducat** recommend a “one use” plastic mold in a two head imprinter, spin on UV imprint material, and direct imprint on wafer above room temperature. The user must deal with system complexity, and no overlay. Their solution offers potential process simplicity but unknown process margin, and potential robustness to particles on wafers.

There are many other vendors selling research tools. They do not appear to be specifically engaged in developing solutions for LED production. The complete processes including substrate should be compared for mold life and critical dimension control as part of an imprint marathon test. The key to success at this stage is to minimize technical risks by making conservative decisions that yield working parts. Fully utilized factories are several years away and the processes can be simplified and cost reduced as volume in the factory builds.

### 8. Clean and Coat Suppliers

Incoming wafers must be cleaned before imprint. Typical cleaners produce wafers with less than 10 particles greater than 0.1 um per wafer. These wafers will produce wafers with no visible defects. Cleaners and coaters are “workhorse” tools in semiconductor processing offered by many vendors; and range from multimillion dollar linked systems for sub micron scanners, to simpler automated tools that sell for $100K to $200K supplied by much smaller companies, and everything in between. A few suppliers will be profiled here.

Both Suss and EVG supply cleaners, coaters and mask aligners to the compound semiconductor market and have a significant installed base in LED manufacturers. SSEC supply single wafer dual sided cleaners to LED wafer suppliers and now offer coater and cleaner combinations. S Cubed offer a coat and clean tool with edge grip at every process station. Their web sites detail the product.
9. Etch Suppliers
Etch process steps are required to clear the imprint pattern, any multilayer resist layers, a hard mask silicon dioxide layer on top of the GaN, and 200-300 nm holes in GaN. Everyone would like to avoid the hard mask, unfortunately GaN etch requires a high density ICP chlorine based plasma, which etches organics very rapidly. The resist layer is limited to a maximum of 200 nm and with substrate variation, can be as thin as 50 nm. As a result a hard mask is essential, and a multichamber etcher to support up to 3-4 different gas chemistries is required. Multiple etch gases can be run in one chamber provided the chambers are carefully conditioned between each gas.

There are 2 etch vendors who build multichamber systems and who are actively engaged in developing etch systems for LED applications; Oerlikon (previously Unaxis) and Trion. Their web sites detail their products.

10. Metrology Suppliers
Imprint at these feature sizes have special metrology needs for thickness measurement on <30 nm thick layers, feature profile by SEM or AFM, and defect monitoring that can be supported by used equipment. Used equipment can be used for defect monitoring because although the features are small, they are a part of a regular array and the device performance will only be affected by relatively large defects (1-2 um). Therefore older low resolution defect tools, such as a KLA 2500, can be used as they will detect changes in groups of features as an apparent change in thickness.

11. Costs
It is always a challenge to make COO calculations useful, particularly before real data on throughout and process life is available, and when the cost structure is speculative. To make a useful comparison, this analysis will focus on likely costs in 2-3 years for the different technology options. It is assumed that competitive pressures will drive capital and material costs to be negligibly different. The model will be kept simple so that the underlying drivers can be understood, rather than make a detailed breakdown based on many speculative components. There are 3 elements to COO per wafer which scale differently:

- Depreciated capital costs and allocated fab costs, both of which scale with the number of wafers processed. Assumptions are, capital cost of the complete module $4.4 M, depreciated over 5 year, a nominal throughput 30 wafers per hour, running at 75% utilization 24/7.
- Consumables, such as materials and process gas that are fixed per wafer. Assumptions are 50 c per spun on layer, 25 c for drop dispensed material, $1 for etch gases.
- Mold costs amortized over the life of the mold.

The major variable between the different solutions is the cost of the original mold, and the cost and life of the working mold. The electron beam original costs varies widely with area, address density and writing strategy.
$400 per sq mm will be used. Life of the original is assumed to be the same as the product life. Costs are lower if a 5x5 mm area is patterned by ebeam, and then step and repeat is used to cover a whole wafer, as described by MII\textsuperscript{22}.

For glass working plates MII has reported making masters by S&R and the process life after cleaning in excess of 15,000 imprints and indicated a cost of 10k per working template in a recent publication\textsuperscript{42}. There is no published data on cost and life of plastic working molds, EVG has suggested a budgetary number of >100 imprints for their plastic molds that will be made by the supplier or the user\textsuperscript{24}. The cost per mold is not known, as a benchmark the lowest quality soda lime glass working plates bought in volume are priced around $250 each\textsuperscript{43}. The cost of the one use plastic sheet needs to be less than $1 an imprint for it to be cost competitive.

<table>
<thead>
<tr>
<th>Mold</th>
<th>Cost per wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>ebeam Master 50 mm wafer</td>
<td>$ 785,500.00</td>
</tr>
<tr>
<td>ebeam Master 5x5 mm</td>
<td>$ 200,000.00</td>
</tr>
<tr>
<td>Glass sub master</td>
<td>$ 100,000.00</td>
</tr>
<tr>
<td>Plastic working plate</td>
<td>$ 250.00</td>
</tr>
<tr>
<td>One use sheet</td>
<td>$ 1.00</td>
</tr>
</tbody>
</table>

The COO associated with the mold are shown above and the net COO for some of the various process choices are shown below.

<table>
<thead>
<tr>
<th>Process or part life</th>
<th>Whole wafer thin hard mold, with direct imprint</th>
<th>S&amp;R thin hard mold + direct imprint</th>
<th>Whole wafer one use plastic mold, direct imprint</th>
<th>Whole wafer bi layer plastic mold, direct imprint</th>
<th>S&amp;R thin hard mold + drop dispense + image reversal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capital</td>
<td>$ 5.85</td>
<td>$ 5.85</td>
<td>$ 5.85</td>
<td>$ 5.85</td>
<td>$ 5.85</td>
</tr>
<tr>
<td>Consumables</td>
<td>$ 1.50</td>
<td>$ 1.50</td>
<td>$ 1.50</td>
<td>$ 1.50</td>
<td>$ 1.50</td>
</tr>
<tr>
<td>Mold</td>
<td>$ 2.24</td>
<td>$ 0.89</td>
<td>$ 2.57</td>
<td>$ 3.57</td>
<td>$ 0.69</td>
</tr>
<tr>
<td>TOTAL</td>
<td>$ 9.59</td>
<td>$ 8.04</td>
<td>$ 9.92</td>
<td>$ 10.92</td>
<td>$ 8.79</td>
</tr>
</tbody>
</table>

The costs range from $8-12 per wafer. Halving the number of wafers processed will approximately double the COO to $16 a wafer. The capital costs of the imprinter are the largest component. The cost is ½ the ~$0.01 per mm\textsuperscript{2} cost that can easily be justified for a high output LED.

**Conclusions**

Patterning of LED's is poised to change the brightness of LED's through the use of Photonic Quasi Crystals. Imprint is poised to impact the manufacturing of LED's. There are a number of different process equipment and process variations to choose from, at different levels of development. The key differentiators are mold technology, and process control.

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2. 4% for each surface, 8% from a flat mirrored LED.
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